UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,579	11/09/1999	ALEXANDER G. MACINNIS	36275/SAH/B6	8181

7590 05/08/2002

John A Wiberg
McAndrews Held & Malloy
500 W Madison Street
Suite 3400
Chicago, IL 60661

EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/437,579	Applicant(s) MACINNIS ET AL.	
	Examiner Kee M Tung	Art Unit 2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-24,29-59,61 and 62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-24,29-59,61 and 62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed 2/27/02 has been considered in preparing this office action.

Claim Rejections - 35 USC § 112

2. Claim 59 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 59 depends on canceled claim 25.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1, 2, 5, 19 and 62 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ben-Yoseph et al (5,949,439).

Ben-Yoseph et al teaches a graphics accelerator (Fig. 1) comprising a data SRAM memory (SRAM 146) for storing graphics data, the graphics data including pixels; a coprocessor (106) for

performing vector operations on a plurality of components of a pixel of the graphics data (col. 3, lines 11-39), wherein the coprocessor processes the plurality of components of the pixels in parallel as elements of a vector (col. 3, line 31 through col. 4, line 7, specially, col. 3, lines 50-56). Therefore, at least claims 1 and 2 are anticipated by Ben-Yoseph et al.

As per claim 5, Ben-Yoseph et al teaches the plurality of components of each pixel, comprise R, G and B components of RGB formatted graphics data (inherent by any 3D graphics pixel data which normally in RGB format or YUV format for video data).

As per claim 19, Ben-Yoseph et al teaches the coprocessor has an instruction set that includes a special instruction for comparing between each element of a pair of 3-element vectors (inherent by the VLIW, col. 3, lines 35-39).

As per claim 62 , Ben-Yoseph et al teaches a DMA engine for transferring the graphics data between the memory and an external memory (col. 4, lines 36-40 and col. 4, line 65 through col. 5, line 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 23, 29-31, 37, 44-46, 50, 51, 58 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439).

The teachings of Ben-Yoseph et al are given in previous paragraph of this office action. However, Ben-Yoseph et al fails to explicitly teach the DMA engine moves data between the local memory and the external memory while the graphics accelerator is using the memory for its load and store operations. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the teachings of Ben-Yoseph et al as claimed because Ben-Yoseph et al teaches the multimedia processor 106 operates under control of a **real time multitasking kernel** and **simultaneously** addresses the five semi-independent, quasi-specialized execution units 152; **transmits and receives data simultaneously** over a high speed RAMbus bus DRAM channel I/O bus and other buses, no wait to send and received data between peripherals, the system bus, or the Rambus DRAM 110 (col. 3, lines 40-56 and col. 5, lines 34-40) and Ben-Yoseph et al further suggests the SRAM 146 is **multiported** (simultaneously or concurrently access to a multiport SRAM is considered an inherent feature of the multiport memory) with connections to the system bus 104, the RAMbus DRAM memory 110 via a 500 Mbyte/s Rambus interface 111, the 792 bit internal data path 109 ... (col. 5, lines 50-62) which can be considered as claimed. Therefore, at least claim 23 would have been obvious by Ben-Yoseph et al for the reasons set forth above.

Claim 29 is similar in scope to claim 23, and additionally requires the graphics accelerator is working on operands and producing outputs for one set of pixels, while the DMA engine is bringing in operands for a future set of pixel operations which would have been obvious (by the

simultaneous operations of Ben-Yoseph et al) for the same reason set forth above with respect to claim 23.

Claim 30 is similar in scope to claim 23, and additionally requires concurrently transferring blocks of unprocessed data and processed data between the main memory and the local memory while the block of graphics data is being processed which would have been obvious (by the simultaneous operations of Ben-Yoseph et al) for the same reason set forth above with respect to claim 23.

The method claim 31 is similar in scope to the apparatus claim 5, and thus is rejected under similar rationale.

As per claim 37, Ben-Yoseph et al teaches each of the plurality of pixels of graphics data comprises YUV components of YUV formatted graphics data (col. 5, lines 5-7).

Claims 44-46 are similar in scope to claim 1 and 19, and thus are rejected under similar rationale.

Claims 50, 51 and 58 are similar in scope to claims 23, 2 and 29, and thus are rejected under similar rationale.

Claim 61 is similar in scope to claim 30, and additionally requires transferring third block of processed graphics data from the on-board memory to the main memory while the first block of graphics data is being processed (obvious by the teachings of Ben-Yoseph et al since Ben-Yoseph et al teaches simultaneously transmits and receives data between peripherals, the system bus or Rambus DRAM, col. 3, lines 40-56).

7. Claims 53-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439) as applied to claims 30 and 50 above, and further in view of Priem et al (6,092,124).

The teachings of Ben-Yoseph et al are given in previous paragraph of this office action. However, Ben-Yoseph et al fails to explicitly teach the DMA engine includes a queue to hold a plurality of DMA commands. This is what Priem et al teaches (Fig. 2, DMA 30 and col. 4, lines 35-59; Priem et al further suggests that the DMA engine 30 can be as part of the I/O unit 16 or I/O device col. 4, lines 35-38, such as, graphics accelerator 18, col. 3, lines 51-56). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Priem et al into the system of Ben-Yoseph et al in order to facilitate the transfer of data for accomplishing rapid writing as taught by Priem et al (col. 4, lines 35-40). Therefore, at least claim 53 and 55 would have been obvious..

As per claim 54, Ben-Yoseph et al teaches the queue comprises a mechanism that allows the graphics accelerator to determine when all the DMA commands have been completed (read and write pointers 136 and 138, col. 5, lines 26-30).

As per claim 56, Ben-Yoseph et al teaches the plurality of DMA commands are executed in the order they are received (inherent by any FIFO buffer and/or software queue 144).

As per claim 57, Priem et al teaches the queue is four deep for storing up to four DMA commands (at least would be obvious by the DMA register, col. 4, lines 39-51).

8. Claims 24 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439) in view of Gulick et al (5,758,177).

The teachings of Ben-Yoseph et al are given in previous paragraph of this office action. However, Ben-Yoseph et al fails to explicitly suggest the external memory is a unified memory that is shared by a graphics display system, a CPU and other peripheral devices. This is what Gulick et al teaches (col. 6, lines 39-47 and Fig. 7, 110). Gulick et al further teaches a multimedia processor (Fig. 2) comprising a video/graphics engine (202), general purpose DSP (206), DMA engine (236), memory buffer (234), an audio engine (204) ... It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Gulick et al into the system of Ben-Yoseph et al in order to provide an unified memory architecture system and thus to fully utilize of the memory capacity and reduce over all system cost without the lost of performance. Therefore, at least claims 24 and 52 would have been obvious by Ben-Yoseph et al and Gulick et al.

9. Claims 6-18, 20-22 32-36, 38-43 and 47-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439) in view of Hancock (5,604,514).

The teachings of Ben-Yoseph et al are given in previous paragraph of this office action. However, Ben-Yoseph et al fails to explicitly mention the pixels are in an RGB16 format. Ben-Yoseph et al teaches receiving video data in an 16-bit YUV format. It was old and well known and well use in the art that the pixel data can be any format, such as, RGB16, RGB8, RGB24, YUV8, YUV16, or YUV24 etc ... Furthermore, Hancock teaches the pixel data can be RGB16, YUV16,

etc ... (Fig. 3, col. 3, line 52 through col. 4, line 6, col. 5, lines 6-17). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Hancock into the system of Ben-Yoseph et al in order to improve video subsystem for concurrently displaying graphics and image data as taught by Hancock (col. 2, lines 28-30). Therefore, at least claims 6-8 and 13-16, would have been obvious by Ben-Yoseph et al, Gulick et al and Hancock.

As per claim 9, Ben-Yoseph et al teaches the two pixels are respectively selected by two special load instructions (col. 3, lines 57-65).

As per claim 10, Ben-Yoseph et al teaches the two special load instructions are for loading a left one and a right one of the two pixels, respectively (150 and col. 3, lines 35-65).

As per claim 11, Ben-Yoseph et al teaches the coprocessor comprises an input register (SRAM 146).

As per claim 12, the combined system fails to specifically suggest the RGB components are expanded into 8-bit components through zero expansion when loaded into the input register. How, it would have been obvious to one of ordinary skill in the at the time the present invention was made to implement the teachings of MPEG decode of Ben-Yoseph et al and Hancock in order to obtain the claimed feature.

As per claims 17 and 18, Ben-Yoseph et al teaches the two pixels are respectively selected by two special load instructions for extracting a first one and a second one of the two pixels, respectively (150 and col. 3, lines 35-65).

As per claim 20, Ben-Yoseph et al teaches a result register for storing the results of the three comparisons (col. 5, lines 50-62).

As per claim 21, the combined system fails to explicitly teach the results of the three comparisons are used together during a single conditional branch operation. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of using VLIW technology and instruction unit of Ben-Yoseph et al in order to increase system processing performance.

As per claim 22, the combined system also fails to explicitly teach the special instruction is for a greater-than-or-equal-to operation. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Ben-Yoseph et al in order to compare the operands or data.

Claims 32-36, 38-43 and 47-49 are similar in scope to claims 6, 8-10, 14-18, 20, 21, and 22, and thus are rejected under similar rationale.

Response to Arguments

10. Applicant's arguments filed 2/27/02 have been fully considered but they are not persuasive.

Regarding claim 1, applicant argues Ben-Yoseph et al fails to suggest "the coprocessor processes the plurality of components of the pixel in parallel as elements of a vector". The examiner disagrees. Ben-Yoseph et al teaches "meltimedia processor 106 interfaces to a host processor 102

in a multimedia computer system 100 to supply functionality including digital video encoding, decoding and playback accelerator , superVGA2D graphics accelerator, 3D graphics accelerator, ..." (Col. 3, lines 14-20); "the multimedia processor 106 uses a VLIW technology, **vector processing**, and SIMD technology to achieve extensive parallel operation" (col. 3, lines 35-39); "the 792 bit wide internal data path moves up to 8 billion integers per second between hundreds of **ALUs working in parallel** to achieve 2 billion integer operations per second for most functions .. (col. 3, lines 50-56)"; "the multimedia 106 is a single, multiple function, multimedia processor that **performs multiple functions that have conventionally been performed using separate fixed function accelerators for graphics** and audio functions (col. 3, line 66 through col. 4, line 11). Furthermore, it was old and well known in the art that the graphics or video data are corresponding to image pixels and each pixel containing RGB and alpha components of the color vector of that pixel, such as, Joshi et al (5,982,381, col. 3, lines 30-52), Shu et al (5,920,682, col. 1, lines 10-25) and Pan et al (5,727,084, col. 5, lines 14-26). Therefore, the multimedia processor 106 of Ben-Yoseph et al can be considered to suggest or teach the claimed subject matter.

Regarding claims 23, 29, 30 and 61, applicant argues that Ben-Yoseph et al fails to teach "DMA engine that moves data between the local memory and the external memory at the same time the graphics accelerator is using the local memory for load and store operation". The examiner disagrees because Ben-Yoseph et al suggests the SRAM 146 is **multiported** (simultaneously or concurrently access to a multiport SRAM is considered an inherent feature of the multiport memory) with connections to the system bus 104, the RAMbus DRAM memory 110 via a 500 Mbyte/s Rambus

interface 111, the 792 bit internal data path 109 ... (col. 5, lines 50-62). Applicant further argues that the cited area of the specification of Ben-Yoseph et al fails to mention a DMA. Well, the teachings of a DMA is cited with respect to claim 62. The teachings of Ben Yoseph mention under 35 USC 102 is incorporated into the 35 USC 103 rejection. The cited areas are to support the simultaneous and concurrent access of the multimedia processor. Therefore, applicant's arguments are not persuasive.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Responses

12. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

If applicant desires to fax a response, (703) **308-9051(52)** may be used for formal communications or (703) **308-5403** for informal or draft communications.

Please label "PROPOSED" or "DRAFT" for informal facsimile communications. For after final responses, please label "AFTER FINAL" or "EXPEDITED PROCEDURE" on the document.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Inquires

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kee M. Tung** whose telephone number is (703) **305-9660**. The examiner can normally be reached on **Tuesday - Friday** from **6:30 am to 5:00 pm**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark Zimmerman**, can be reached on (703) **305-9798**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) **306-0377**.

Kee M. Tung
Primary Examiner
Art Unit 2671

April 30, 2002